**Module: R3: DLD + DSD**

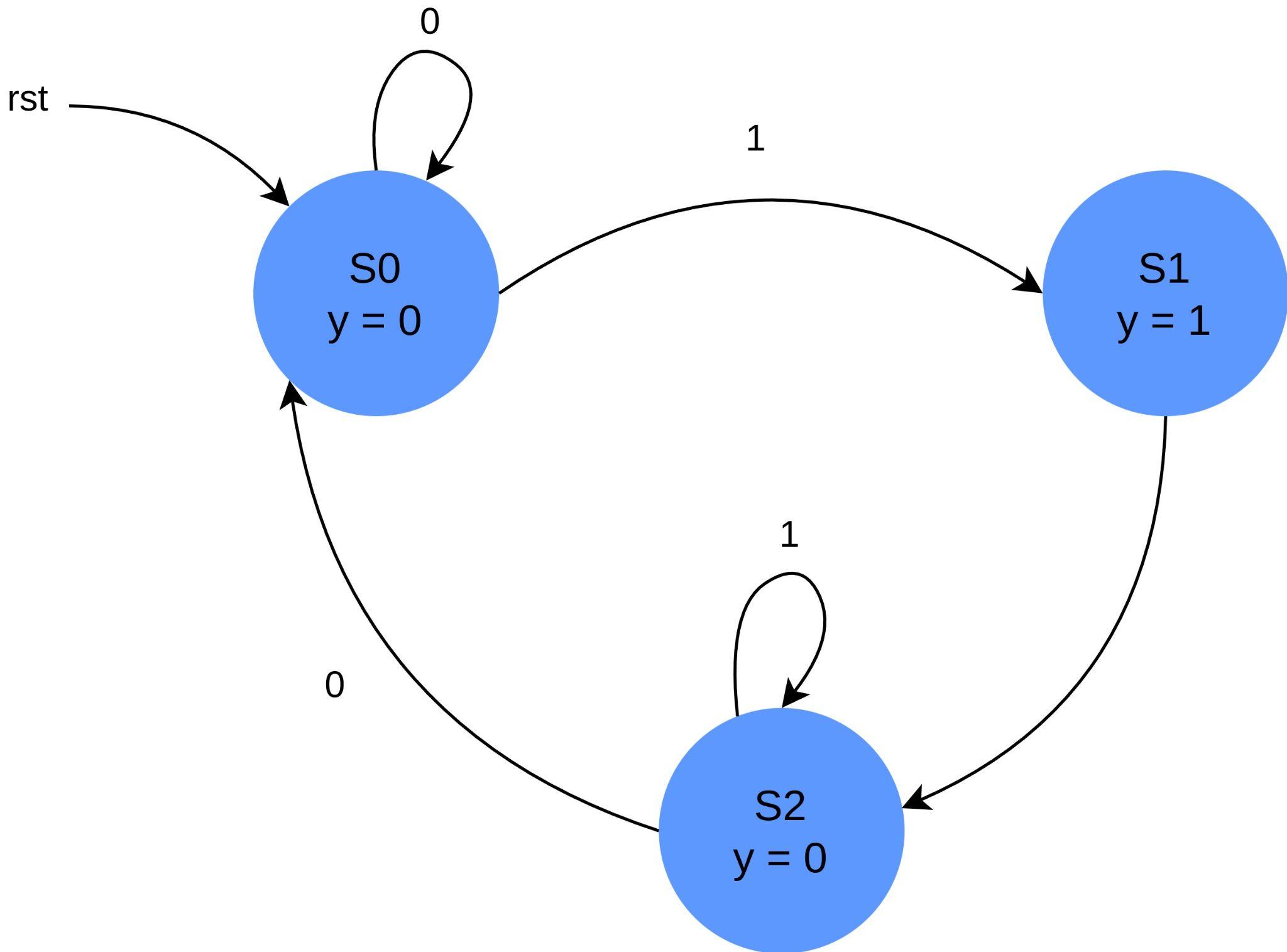
**Section:** Sequential Circuits **Task:** Assignment 2

**Assignment 2**

**Sequential Circuits**

* **Question 1: Design button press synchronizer:**

1. **FSM Diagram:**

****

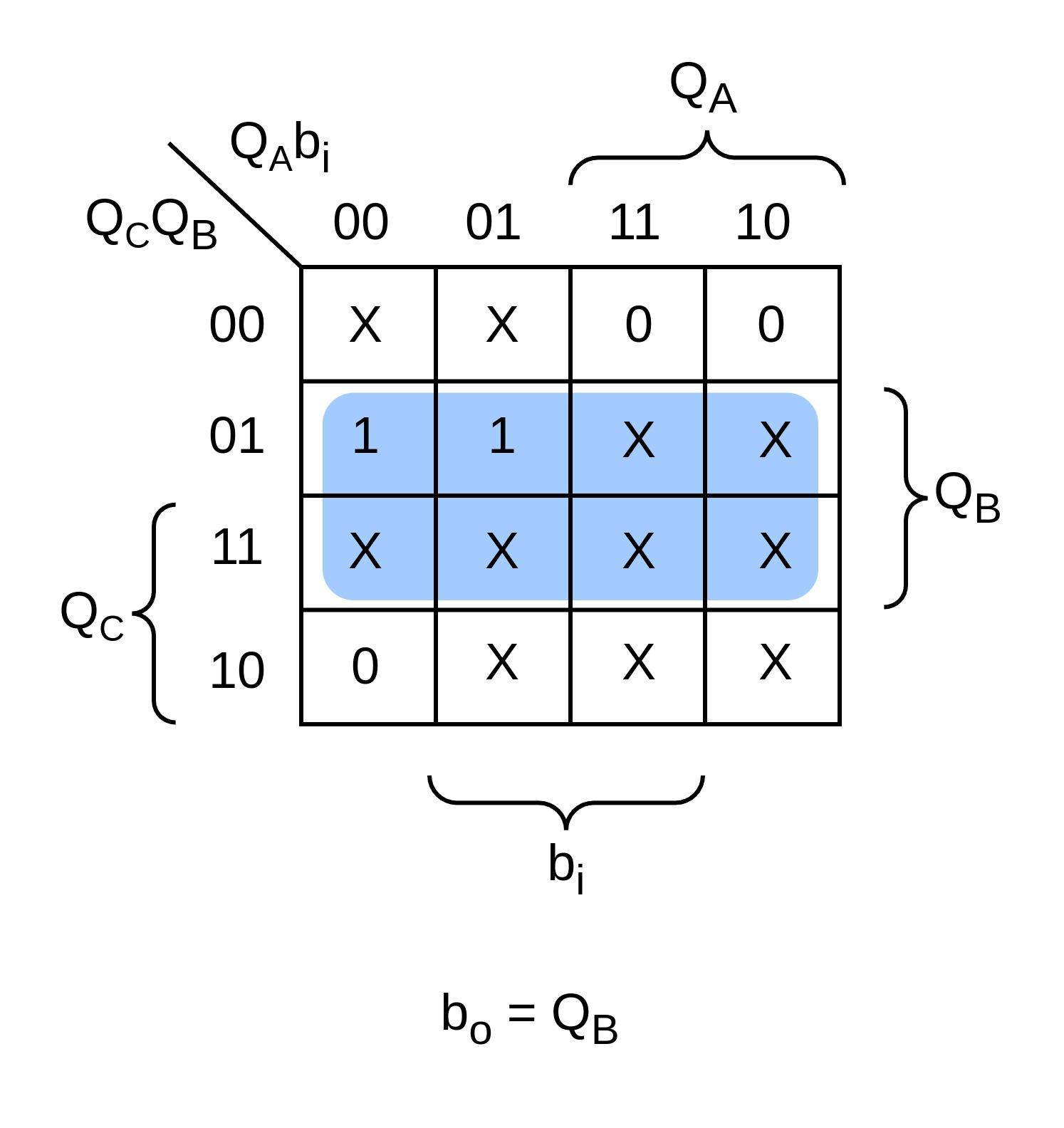
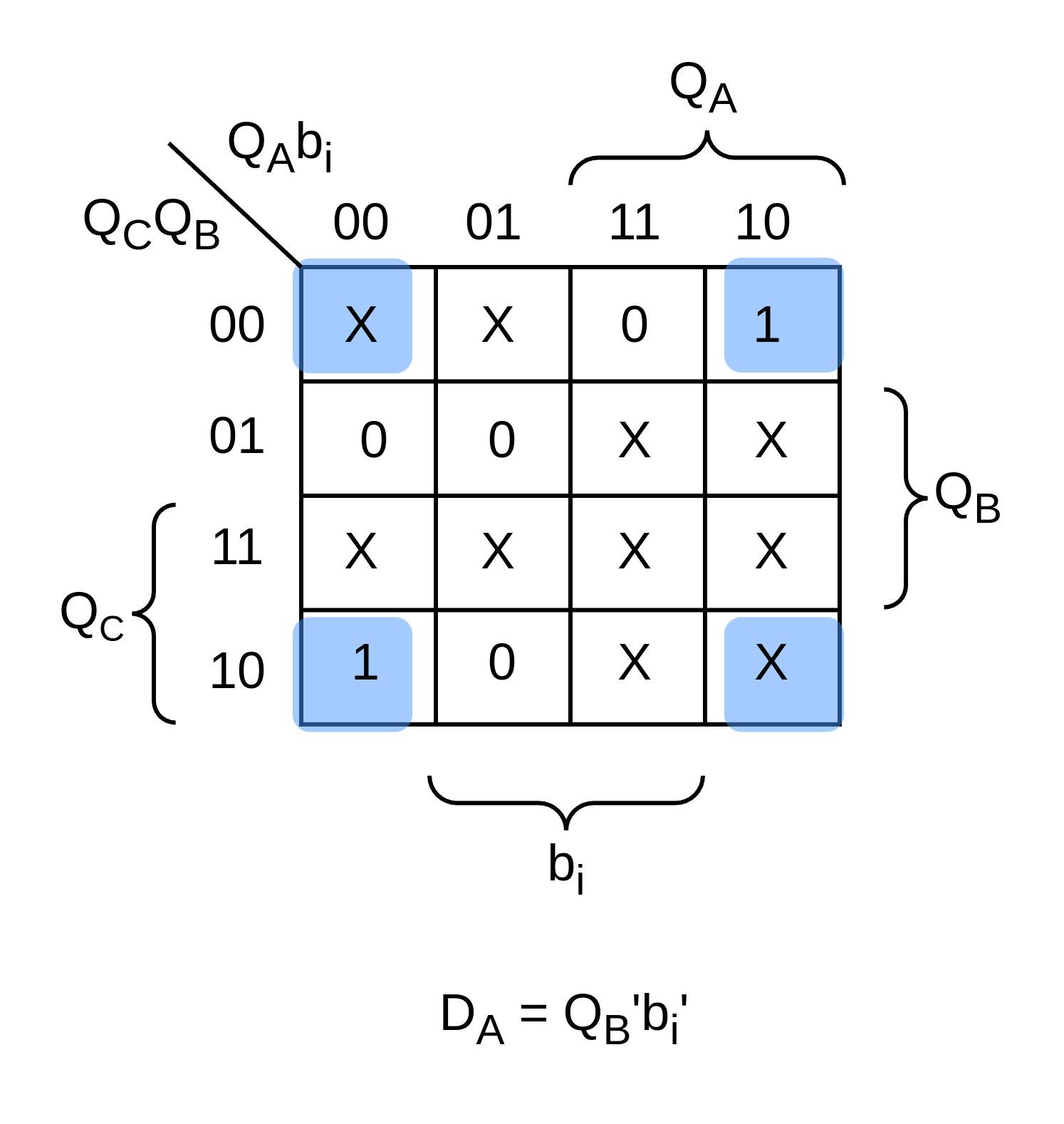
1. **Truth Table:**

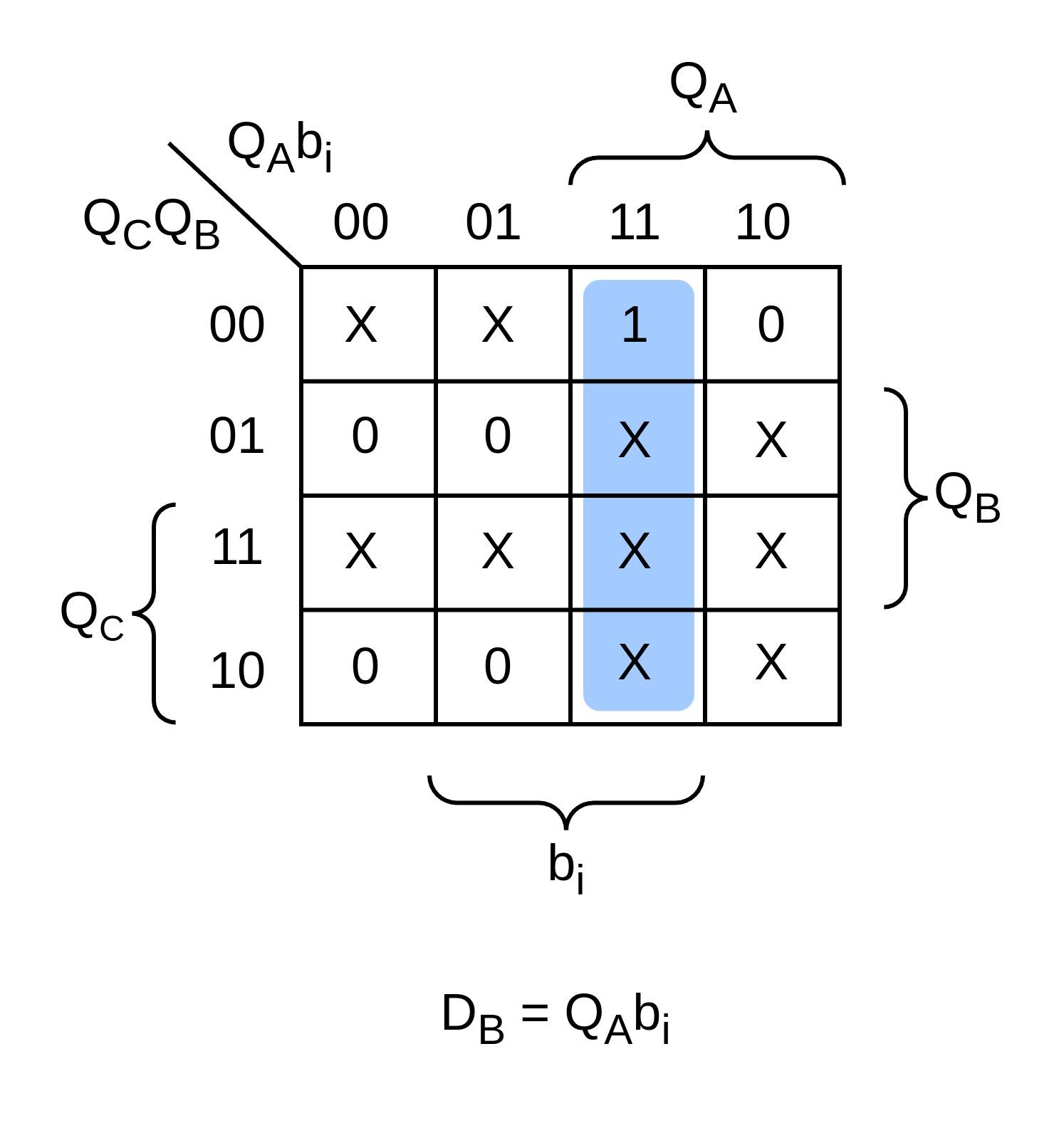
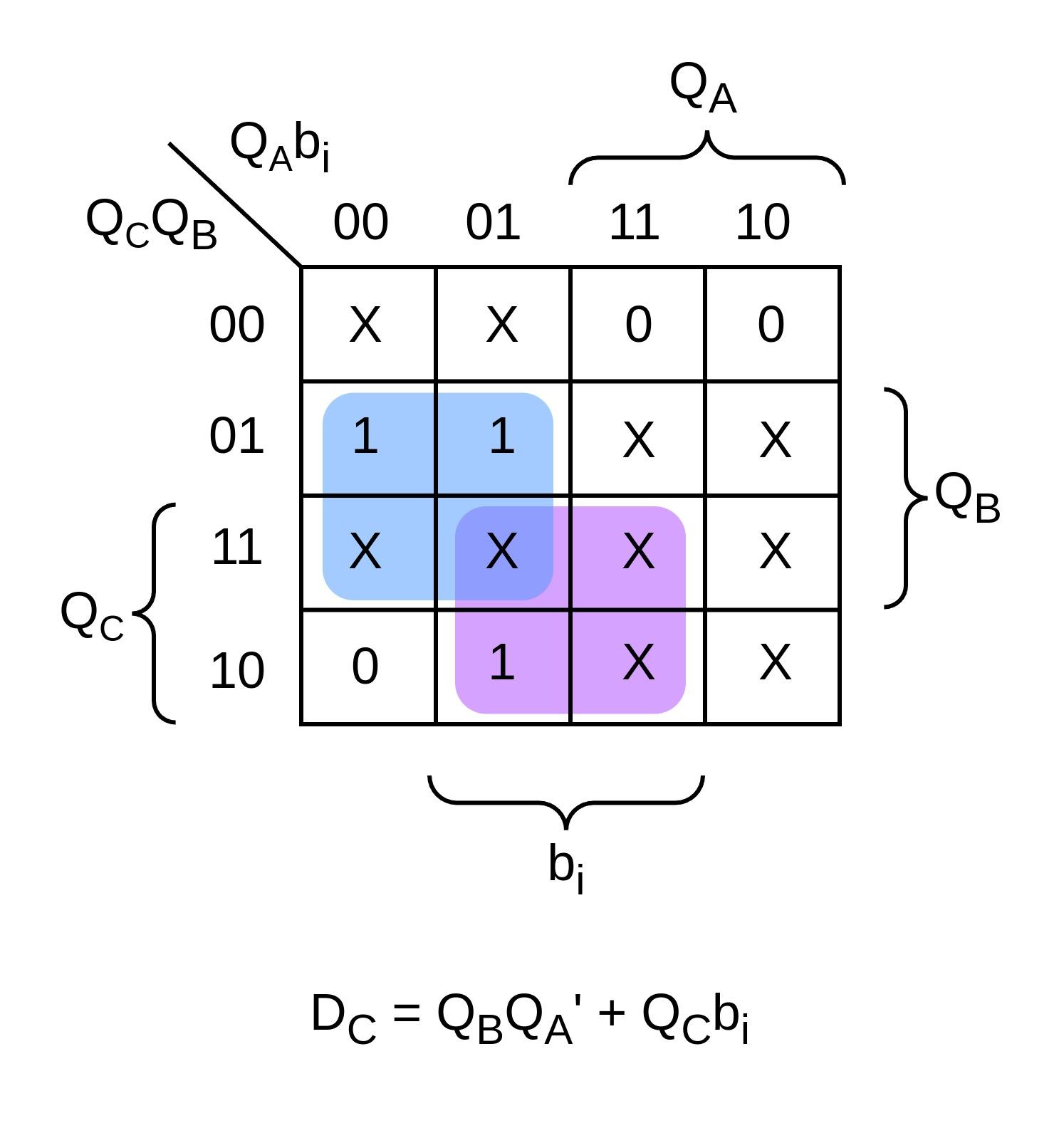
| **One-Hot Encoding** | | **S0 = 001** | **S1 = 010** | **S2 = 100** |
| --- | --- | --- | --- | --- |

| Present State | | | Input | Next State | | | Output | Inputs to Flip-Flops | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| QC | QB | QA | bi | QC+1 | QB+1 | QA+1 | bo | DC | DB | DA |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

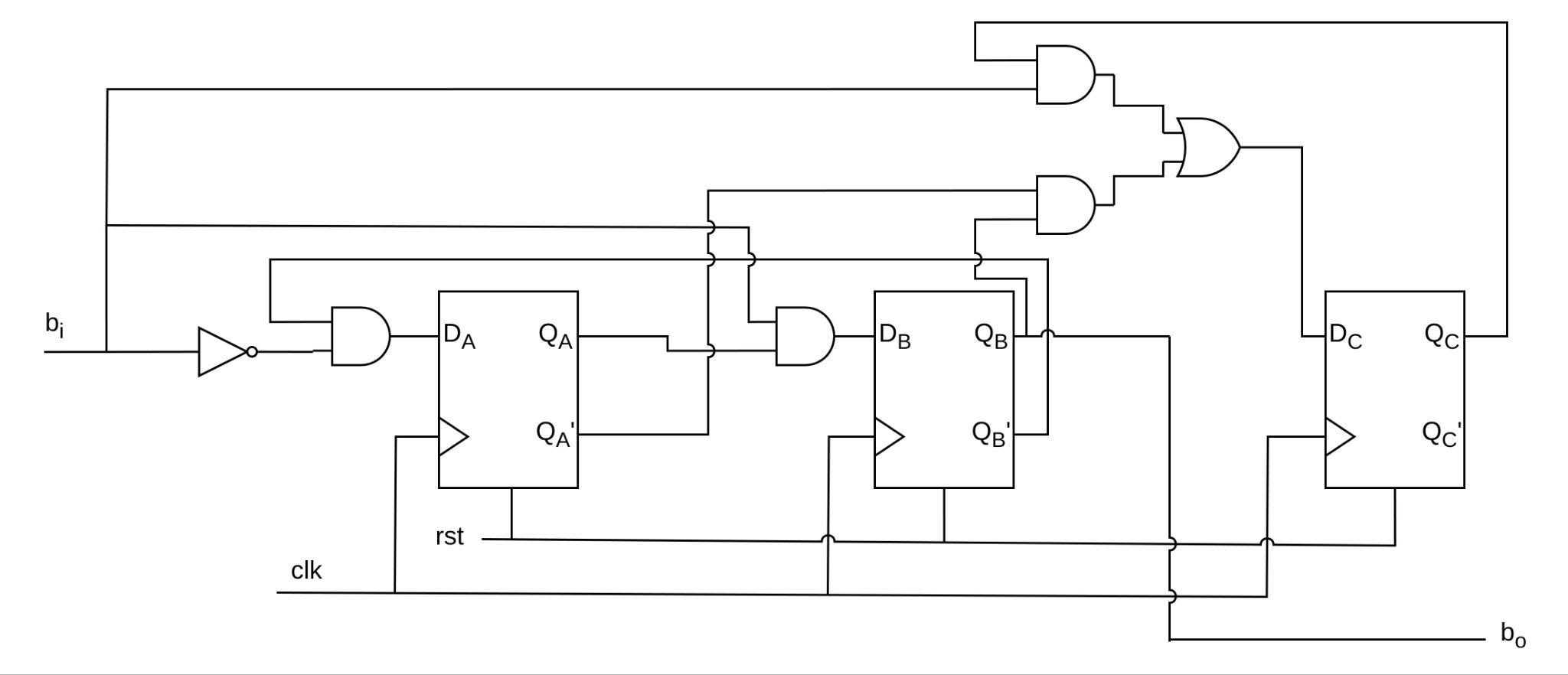
1. **Circuit Diagram:**

Using K-Maps:

Here’s the final circuit:



1. **Verilog Code:**

module button\_press\_synchronizer (input clk, rst, bi, output reg bo);

localparam S0 = 3'b001;

localparam S1 = 3'b010;

localparam S2 = 3'b100;

reg [2:0] state;

always @(posedge clk or posedge rst)

begin

if (rst)

state <= S0;

else

begin

case (state)

S0 : state <= bi? S1 : S0;

S1 : state <= S2;

S2 : state <= bi ? S2 : S0;

endcase

end

end

always @(state)

case (state)

S0 : bo <= 0;

S1 : bo <= 1;

S2 : bo <= 0;

default : bo <= bo;

endcase

endmodule

1. **Testbench:**

module tb\_button\_press\_synchronizer;

reg clk, rst, bi;

wire bo;

button\_press\_synchronizer m1 (.clk(clk), .rst(rst), .bi(bi), .bo(bo));

always #5 clk = ~clk;

initial begin

$dumpvars;

clk = 0;

rst = 0;

bi = 0;

#10;

rst = 1;

bi = 1;

#20

rst = 0;

#30;

bi = 0;

#20;

bi = 1;

#50;

bi = 0;

#10;

bi = 1;

#20;

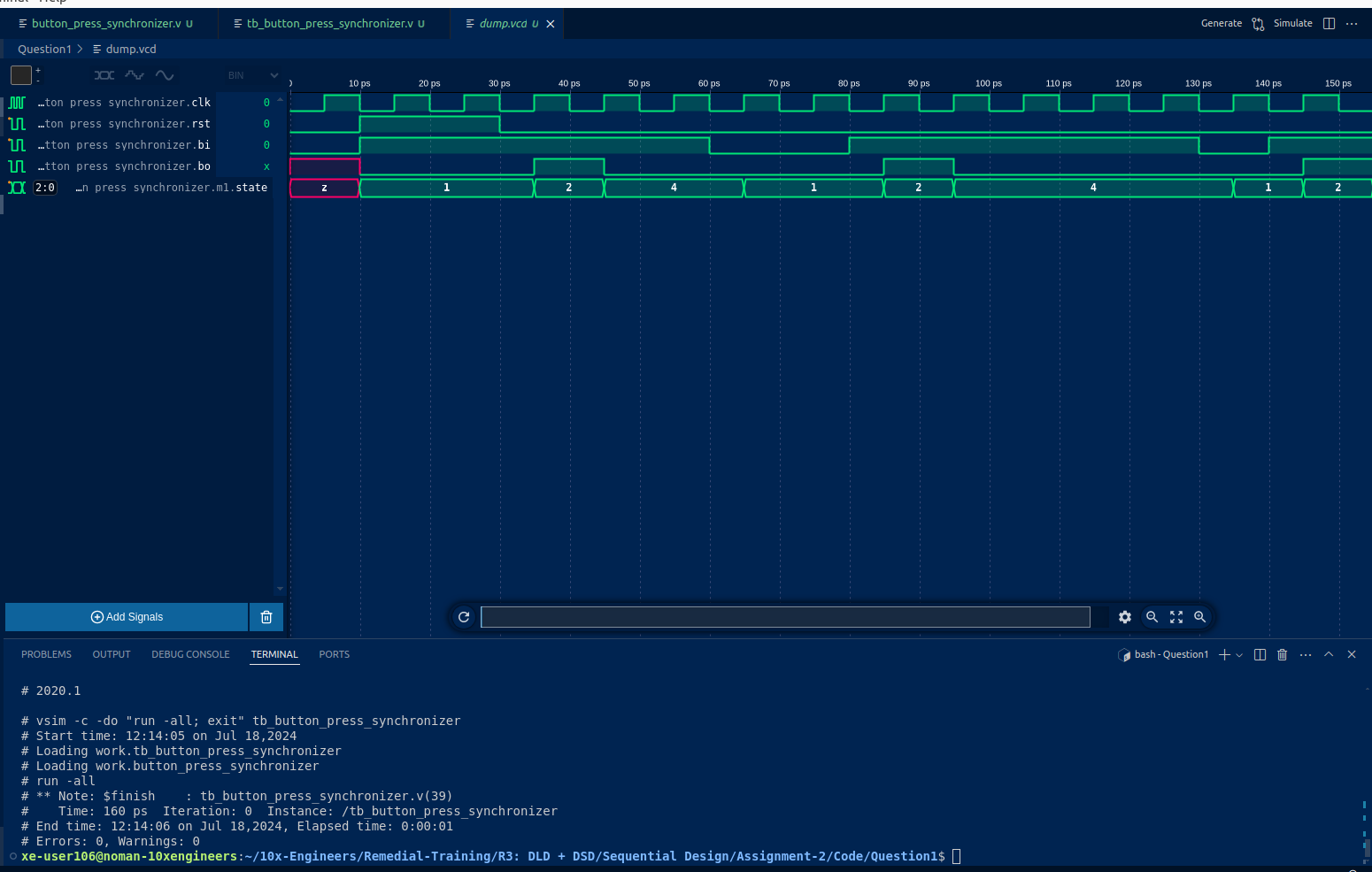
bi = 0;

$finish;

end

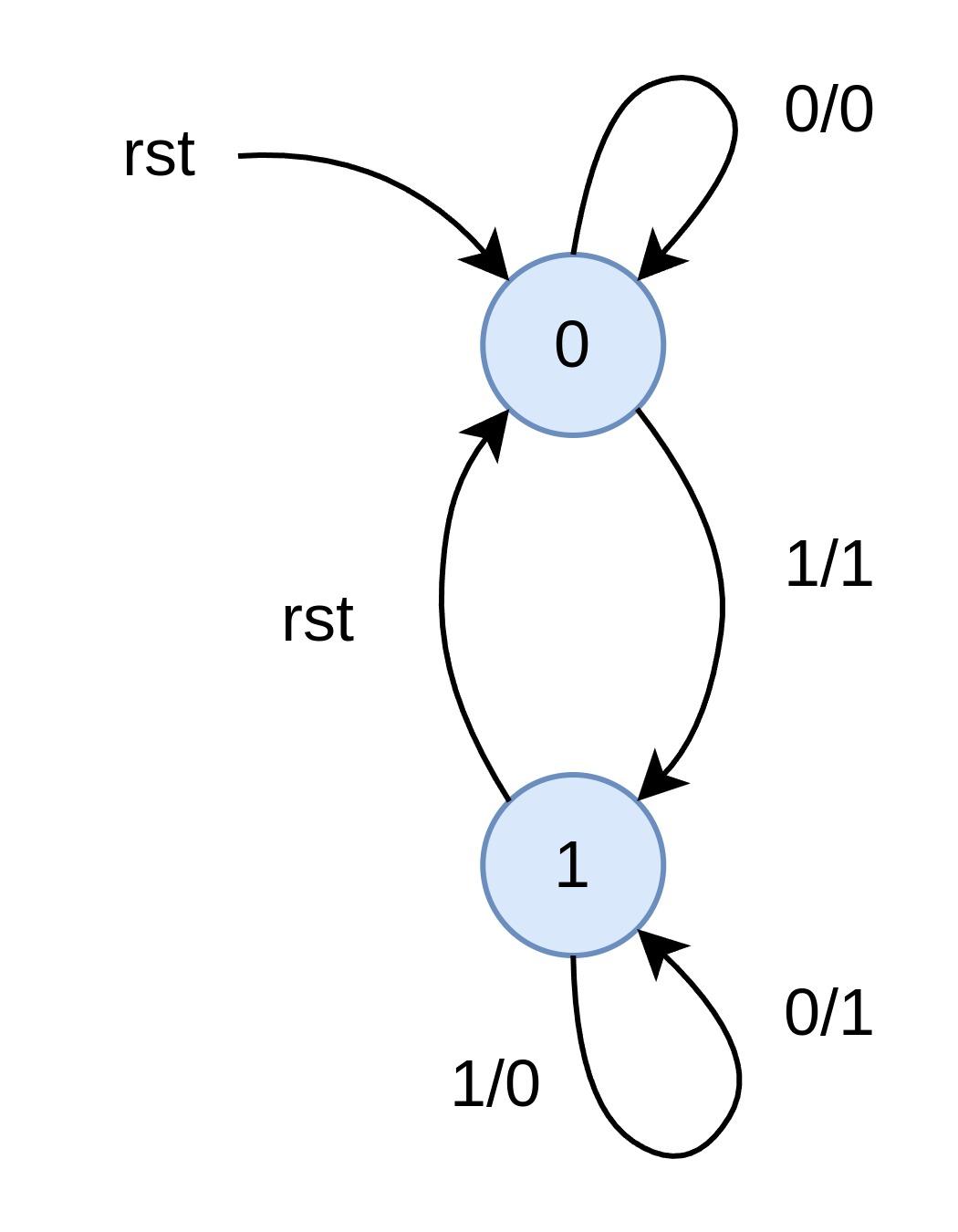
endmodule

1. **Output:**

****

* **Question 2: Serial Input 2’s Complementer:**

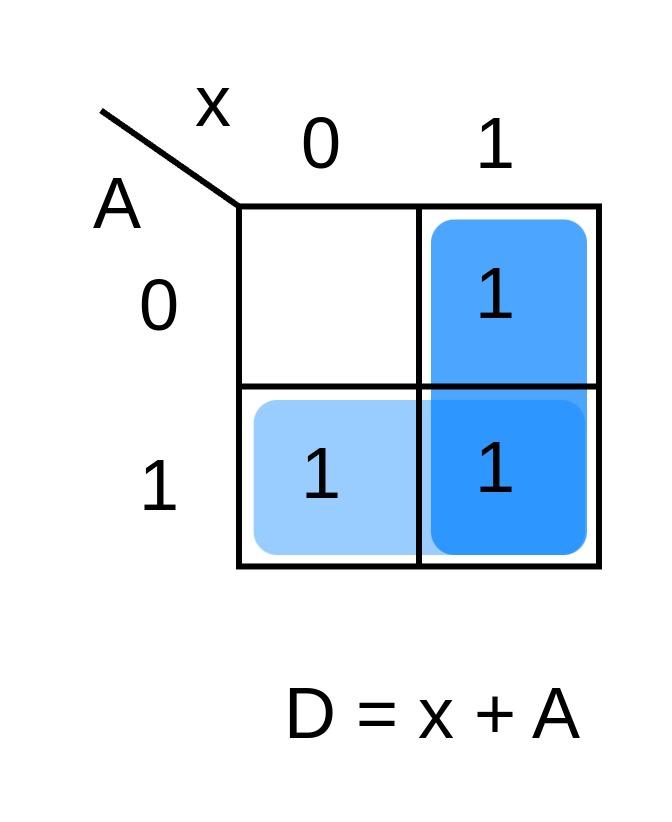
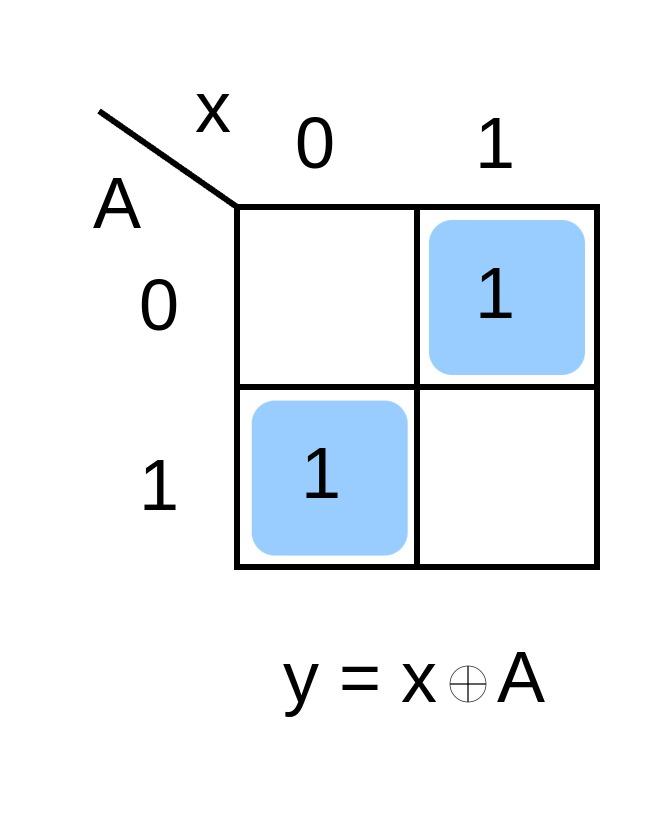
1. **State Diagram:**

****

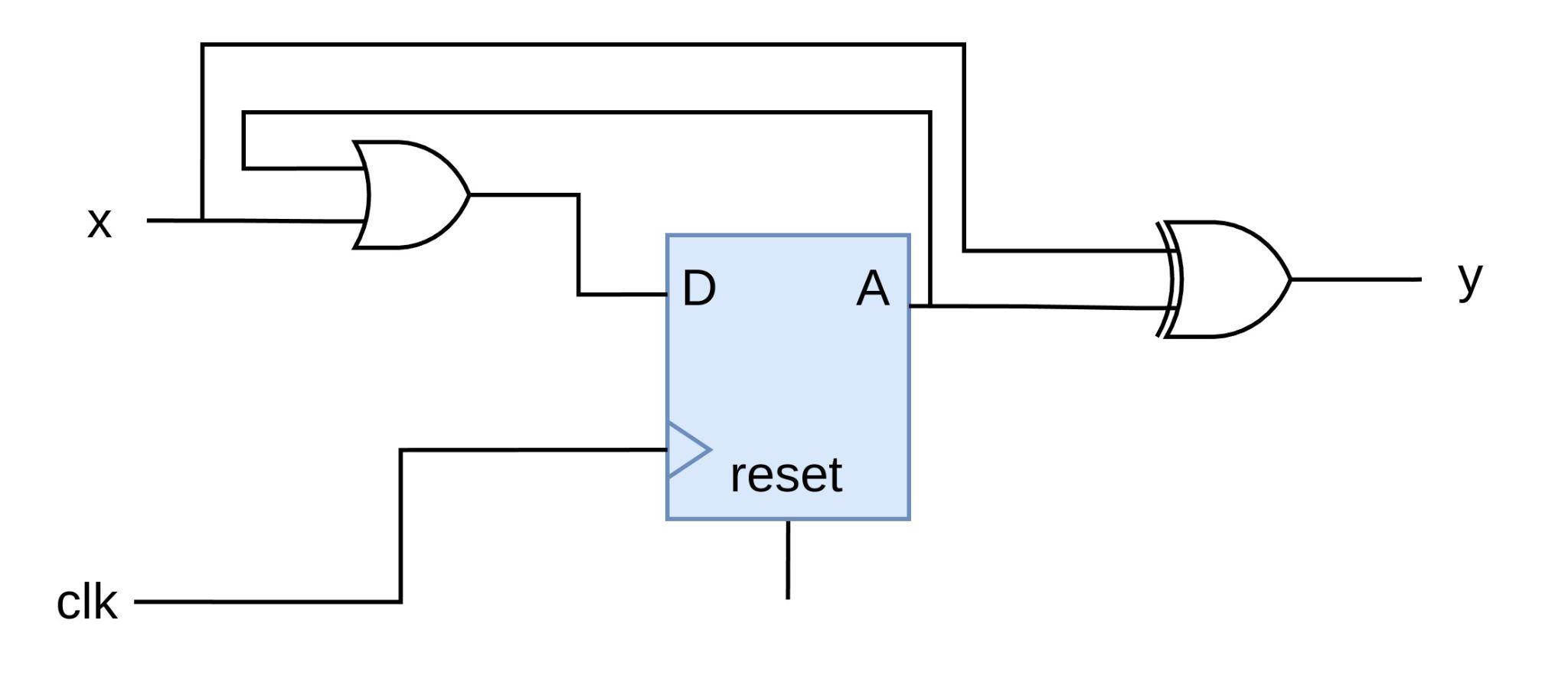
1. **State Table:**

| Present State | Input | Next State | Output | Flip-Flop Input |
| --- | --- | --- | --- | --- |
| Qt | x | Q(t+1) | y | D |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |

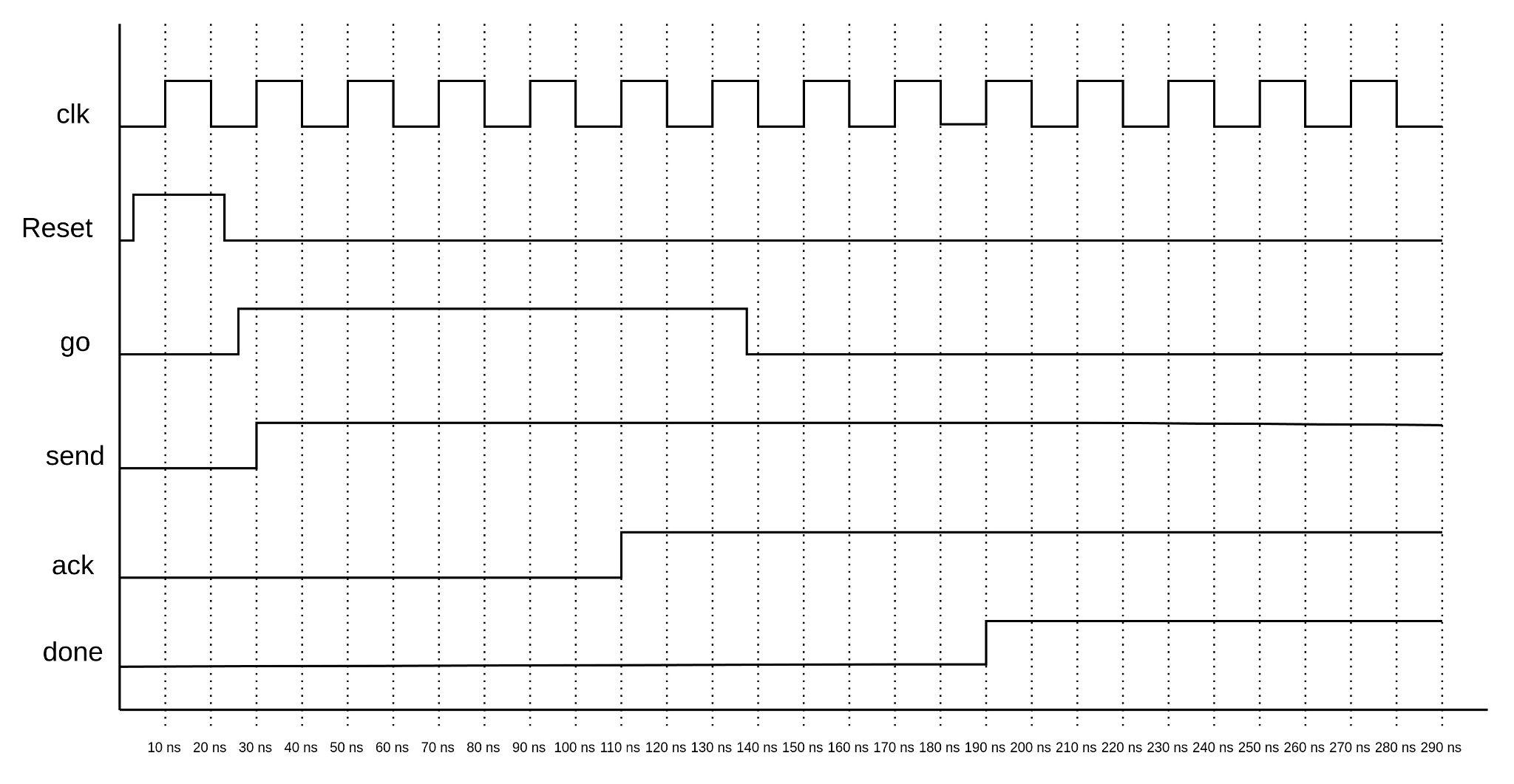
K-maps:

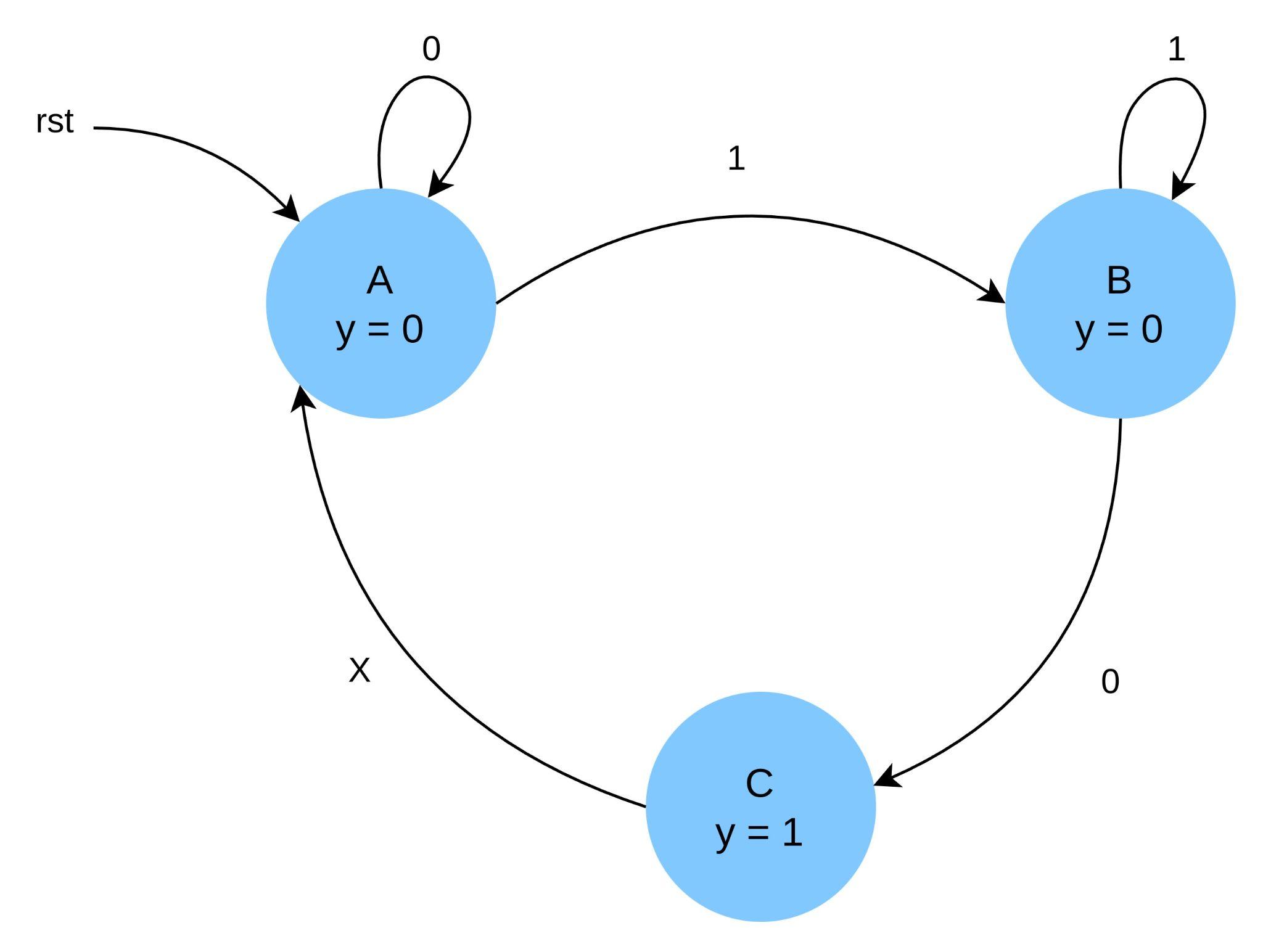
1. **Circuit Diagram:**

****

* **Question 3: Timing Diagram:**

****

* **Question 4: Pulse Detector:**
  1. **FSM Diagram:**

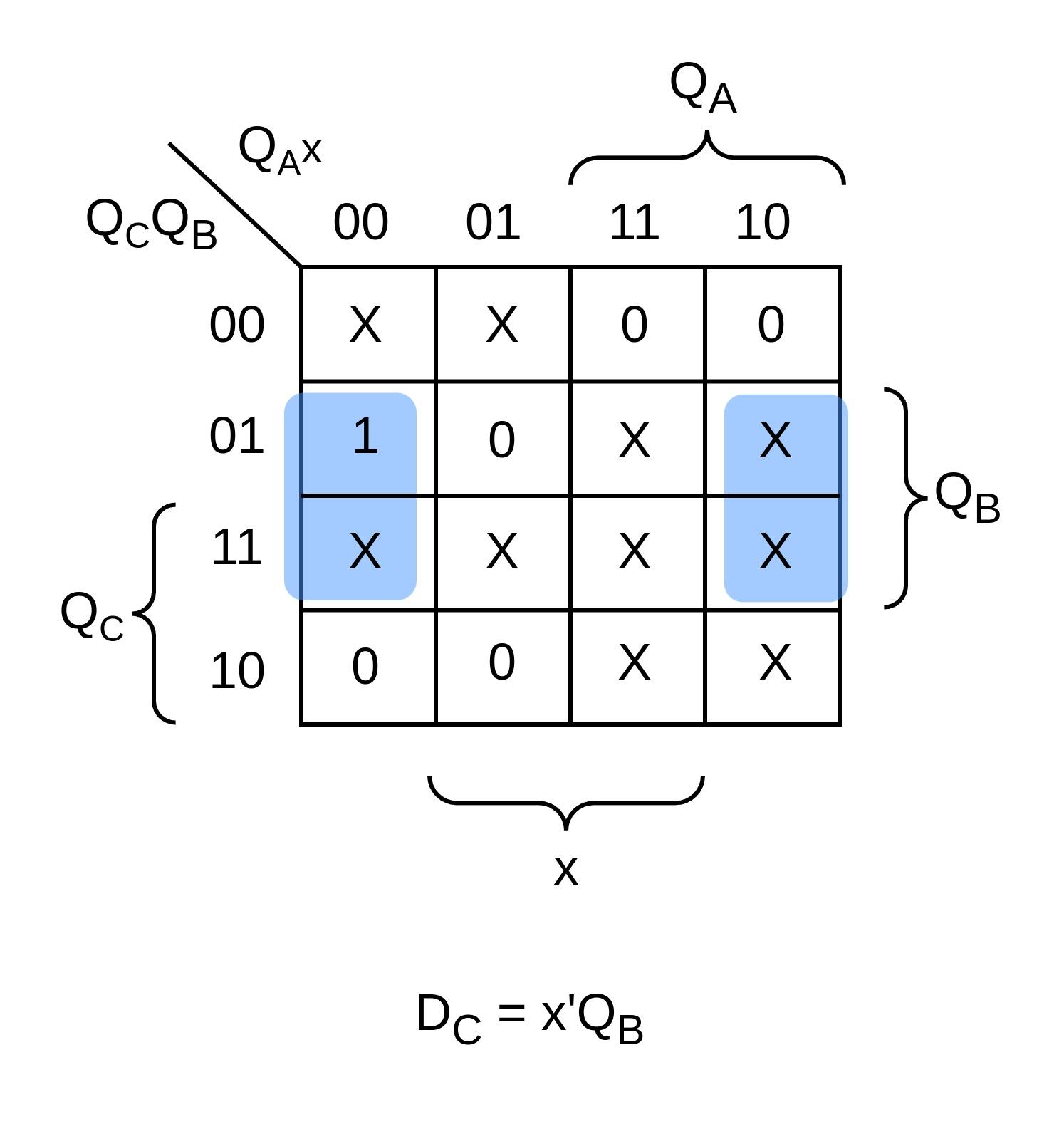
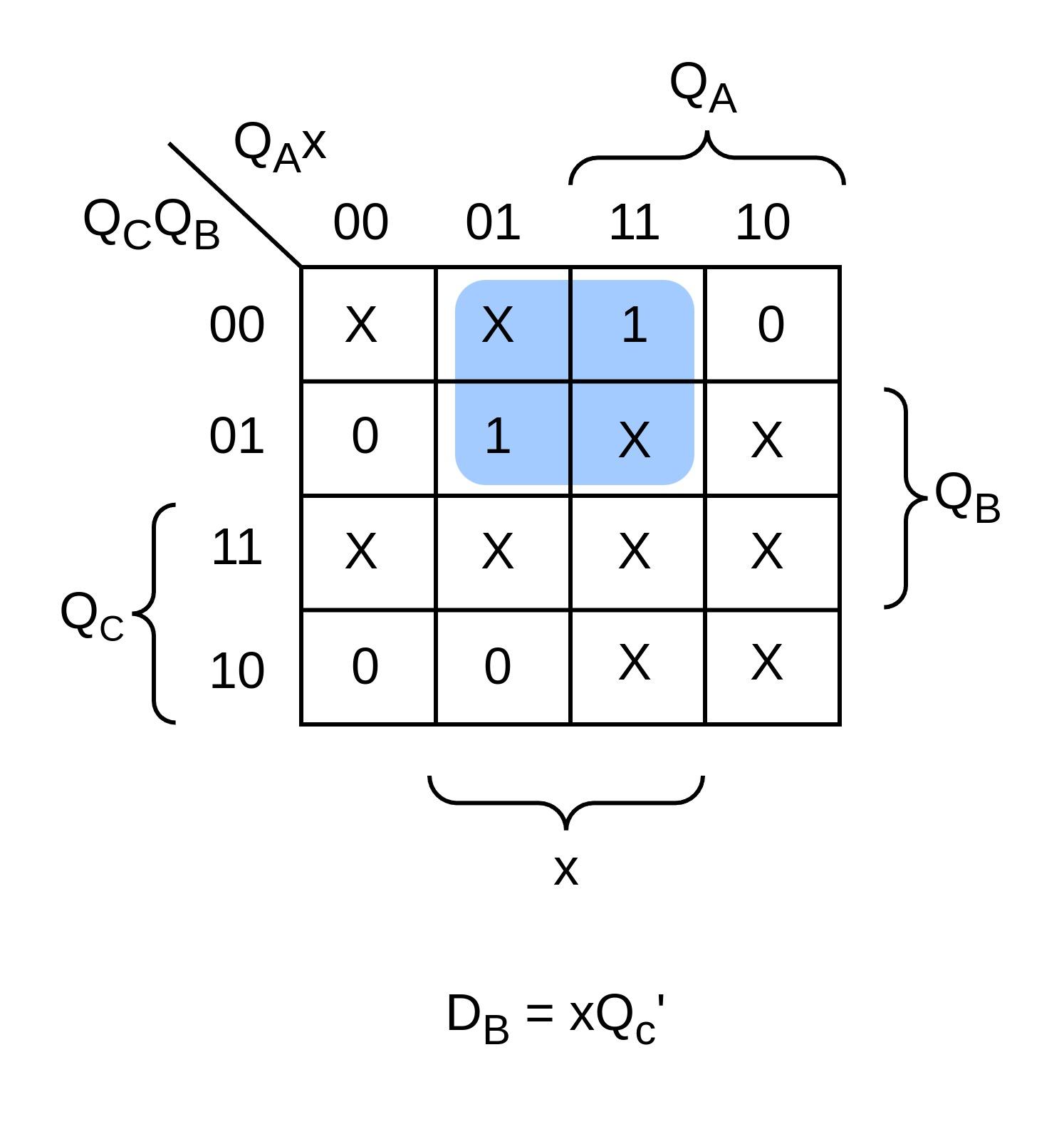
****

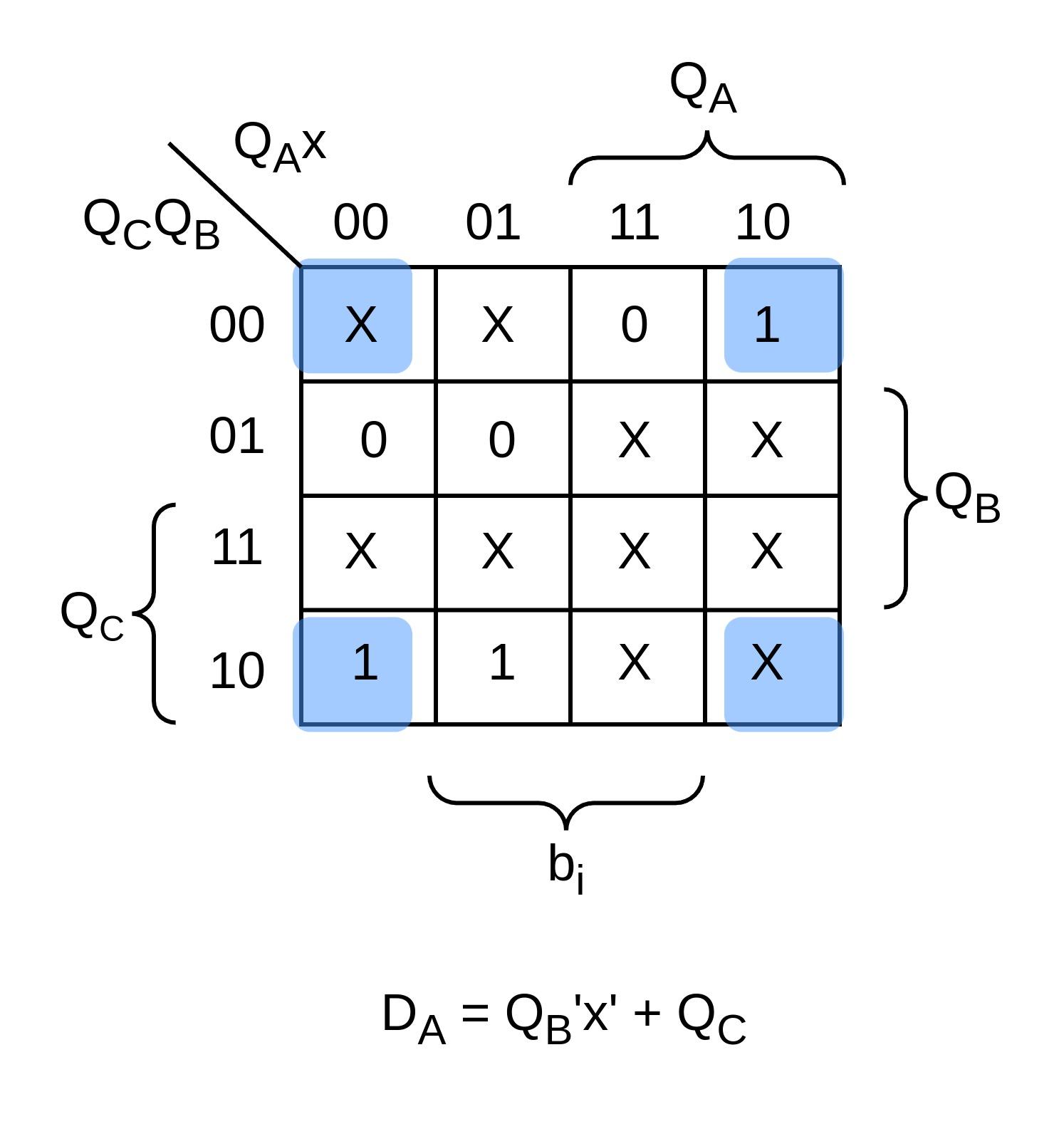
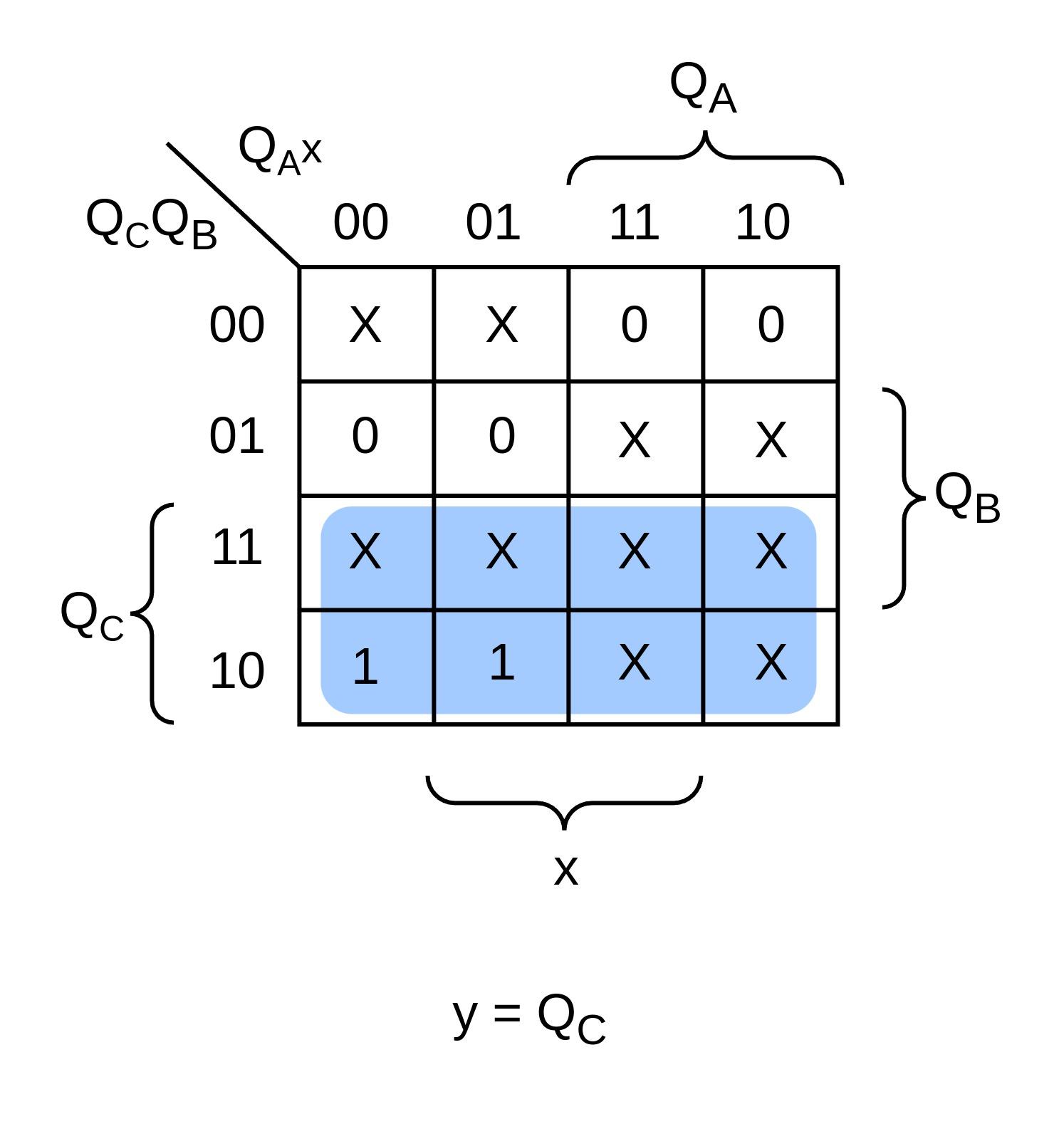
* 1. **Truth Table:**

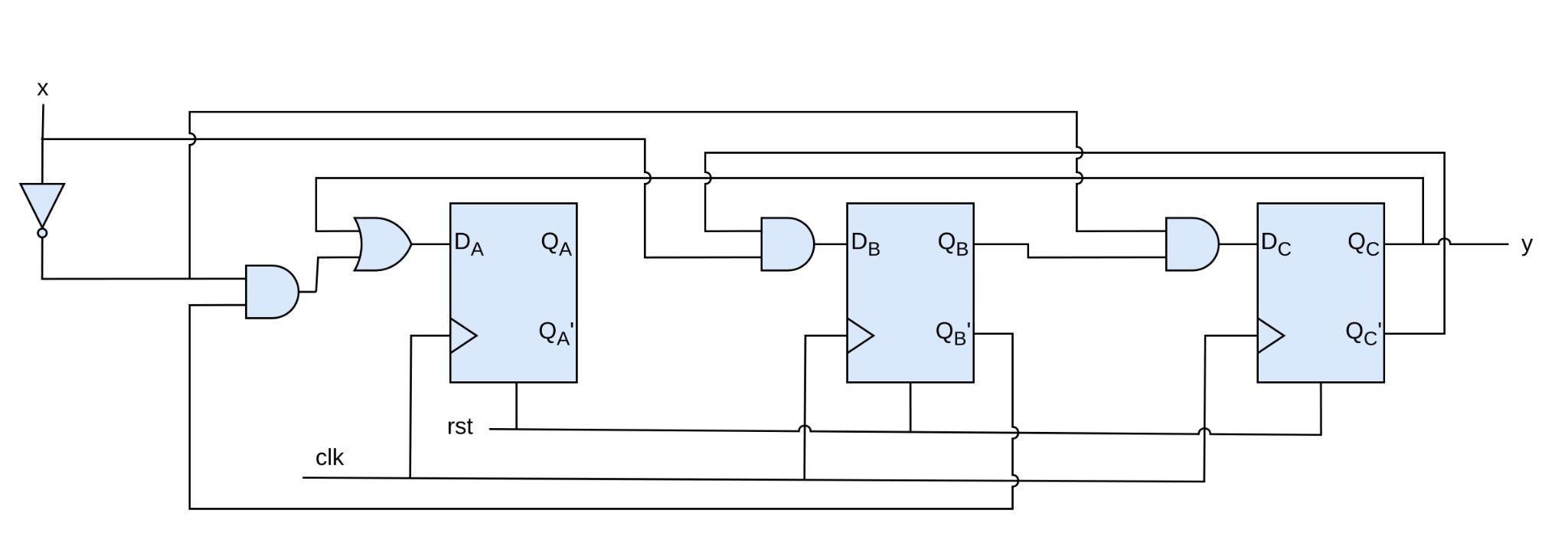
| **One-Hot Encoding** | | **A = 001** | **B = 010** | **C = 100** |
| --- | --- | --- | --- | --- |

| Present State | | | Input | Next State | | | Output | Inputs to Flip-Flops | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| QC | QB | QA | x | QC+1 | QB+1 | QA+1 | y | DC | DB | DA |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

1. **Circuit Diagram:**

** **

** **

****

1. **Verilog Code:**

module pulse\_detector (input clk, rst, x, output reg y);

localparam A = 3'b001;

localparam B = 3'b010;

localparam C = 3'b100;

reg [2:0] state, next\_state;

reg x\_previous;

//State-Transition

always @(posedge clk or rst)

begin

if (rst)

state <= A;

else

state <= next\_state;

end

//Next-State Logic

always @(\*)

begin

case (state)

A :

begin

if (!x)

next\_state <= A;

else

next\_state <= B;

end

B :

begin

if (!x && x\_previous)

next\_state <= C;

else

next\_state <= B;

end

C : next\_state <= A;

default : next\_state <= A;

endcase

end

//Output

always @(posedge clk or posedge rst)

begin

if (rst)

y <= 0;

else if (state == C)

y <= 1;

else

y <= 0;

end

//Detect Falling-Edge

always @(posedge clk or posedge rst)

begin

if (rst)

x\_previous <= 1;

else

x\_previous <= x;

end

endmodule

1. **Testbench:**

module tb\_pulse\_detector;

reg clk, rst, x;

wire y;

pulse\_detector m0 (.clk(clk), .rst(rst), .x(x), .y(y));

always #5 clk = ~clk;

initial begin

$dumpvars;

clk = 0;

rst = 0;

x = 1;

#20;

rst = 1;

#20;

rst = 0;

#10;

x = 0;

#20;

x = 1;

#20;

x = 0;

#30;

x = 1;

#40;

rst = 1;

#10;

x = 0;

#30;

x = 1;

rst = 0;

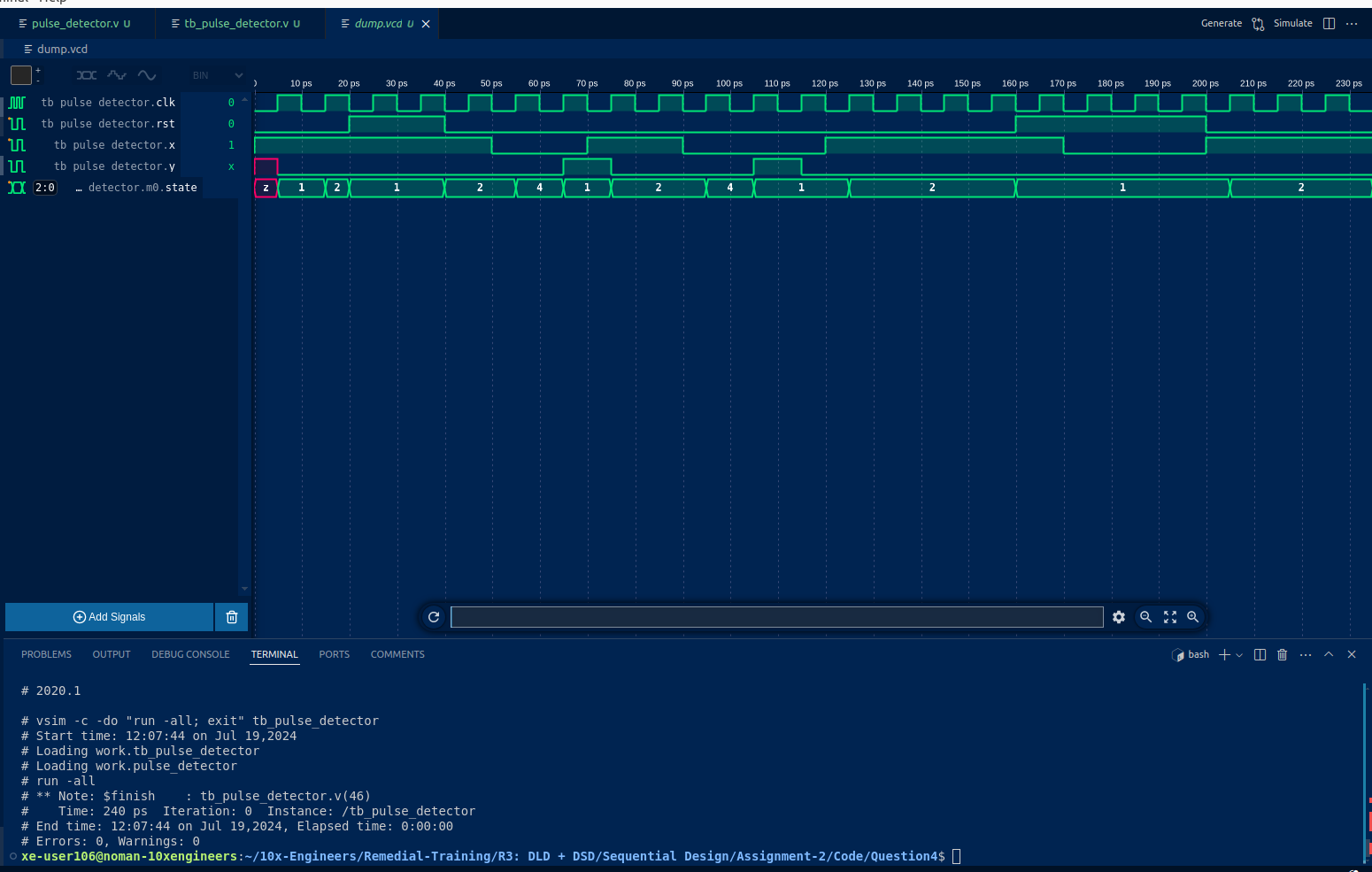
#40;

$finish;

end

endmodule

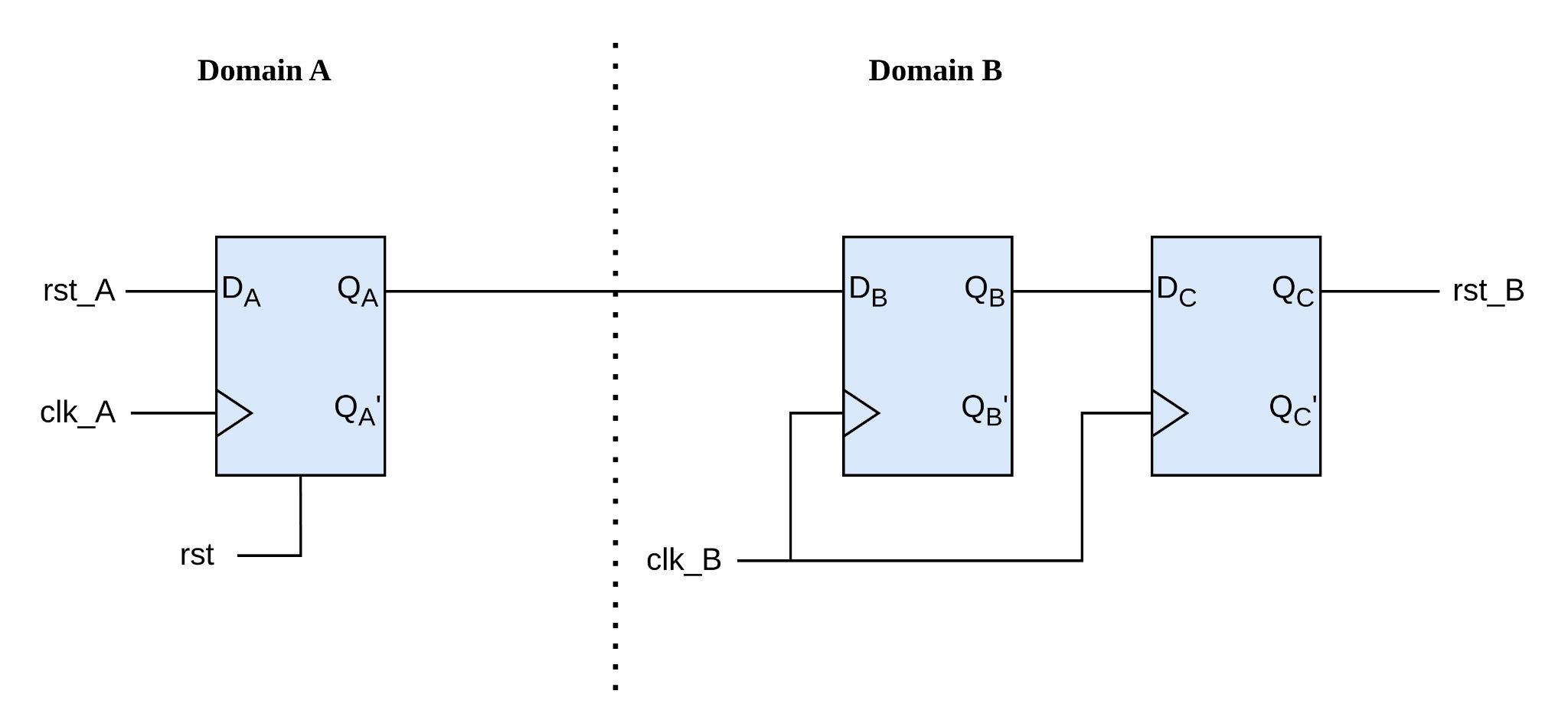
1. **Output:**

****

* **Question 5: Asynhcronus reset:**

Since we are dealing with 2 different clock domains. Hence, in order to avoid any glitches or metastability, I’ll be using a two-flop synchronizer ciruit to map the **reset\_A** signal synchronously with clock of domain B (**clk\_B**)

* 1. **Circuit Diagram:**

****

* 1. **Verilog Code:**

module d\_ff (input clk, rst, d, output reg q);

always @(posedge clk or posedge rst) begin

if (rst)

q <= 1'b0;

else

q <= d;

end

endmodule

module synchronizer (input clk\_A, clk\_B, rst\_A, rst, output reg rst\_B);

wire w0, w1, w2;

d\_ff m0 (.clk(clk\_A), .rst(rst), .d(rst\_A), .q(w0));

//Two Flops Synchronizer

d\_ff m1 (.clk(clk\_B), .rst(1'b0), .d(w0), .q(w1));

d\_ff m2 (.clk(clk\_B), .rst(1'b0), .d(w1), .q(w2));

assign rst\_B = w2;

endmodule

* 1. **Testbench:**

module tb\_synchronizer;

reg clk\_A, clk\_B, rst, rst\_A;

wire rst\_B;

synchronizer dut (.clk\_A(clk\_A), .clk\_B(clk\_B), .rst(rst), .rst\_A(rst\_A), .rst\_B(rst\_B));

always #5 clk\_A = ~clk\_A;

always #20 clk\_B = ~clk\_B;

initial begin

$dumpvars;

clk\_A = 0;

clk\_B = 0;

rst = 0;

rst\_A = 0;

#20;

rst = 1;

#10;

rst\_A = 1;

#40;

rst = 0;

#40;

rst\_A = 0;

#80;

rst\_A = 1;

#20;

rst\_A = 0;

#30;

rst\_A = 1;

#30;

rst\_A = 0;

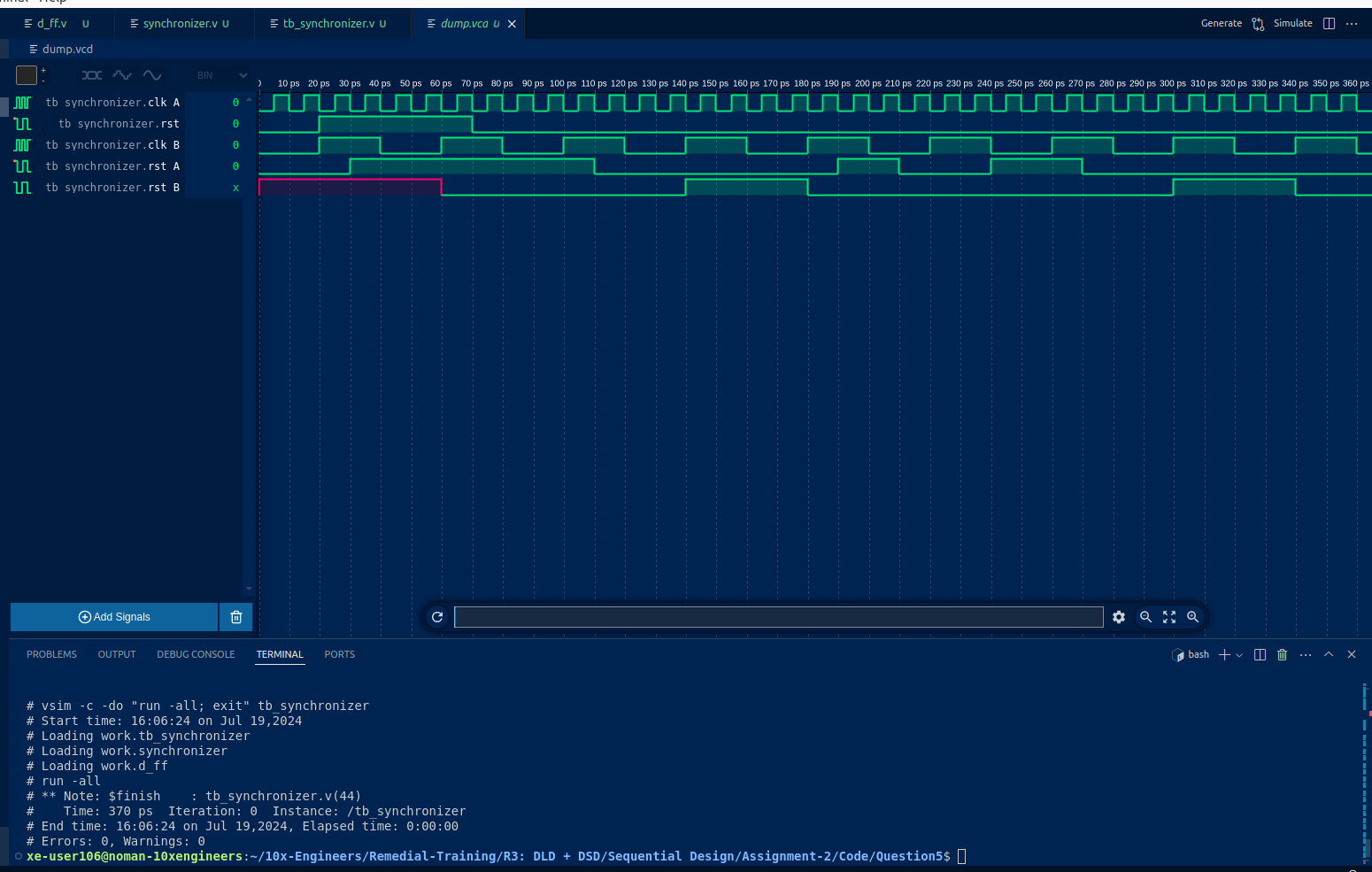
#100;

$finish;

end

endmodule

* 1. **Output:**

****